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Optical PreAmplifier (TIA) Design for High Speed Optical Communication with Optimized Performance

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Abstract:In this paper, the bandwidth enhancement of TIA amplifier can be design for achieving the high information capacity which is used in optical fiber communication for existing transimpedance amplifiers in CMOS technology. The proposed TIA amplifier also trade-offs between gain, bandwidth, noise, and group delay variation with introduce on differential architecture along an RGC network as input and incorporating a feedback network and peaking inductors for bandwidth enhancement. The capacitive degeneration is also introduced to increase the number of zeros for better phase performance.

Keywords: Active feedback, bandwidth extension, broadband, induced gate noise, regulated cascode (RGC), transimpedance amplifier (TIA).

I. INTRODUCTION

The Optical communication technology grows rapidly for high speed telecommunication networks and data communications in recent years[1]. It has one of the cornerstones of today's revolution in information technology. It also has area of interest in high speed optical and electronic devices and systems. Development of faster communication channels was motivated by proliferation of the Internet, high-speed microprocessors, and inexpensive memory in recent years[2]. In addition, optical fibre communication also received immense attraction because of its advantages over electrical communication, such as transmission capacity, low power consumption, high security, low cost, less cross-talk, and lower EMI[3].

II. PROPOSED DESIGN OF TRANSIMPEDANCE AMPLIFIER

Accordingly, the next generation 40 Gb/s optical transmission will be focused on reducing the number of channels to mitigate these issues. In the light of this circumstance, a single channel 40 Gb/s TIA in CMOS technology has been proposed in this work[4,5,6]. The primary challenge of the proposed work is to increase the bandwidth much higher than the existing TIA architectures to minimize the inter-symbol interference (ISI) in 40 Gb/s data rate. In addition, high transimpedance gain, low input referred noise and small group delay variation are parts of design goal. Since total integrated noise of TIA trades with bandwidth, TIA bandwidth is usually designed as 0.7 times bit rate to keep integrated noise as moderate as possible[8,9]. Also, the trade-off between bandwidth and group delay variation makes it extremely challenging to design a TIA in data rate as high as 40 Gb/s.

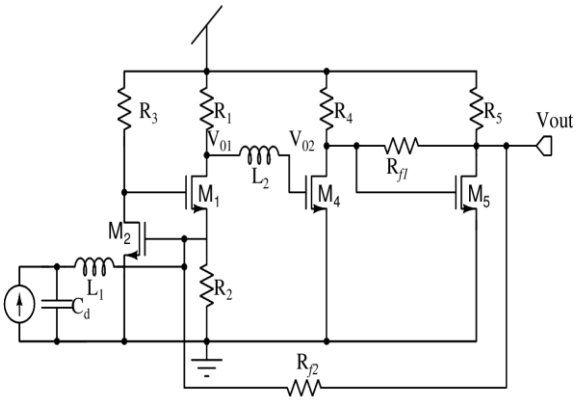

Fig.1 Circuit Diagram for Purposed TIA

A. RGC Network

Regulated cascode (RGC) is widely used for broad-band TIA design in high-speed optical communication.

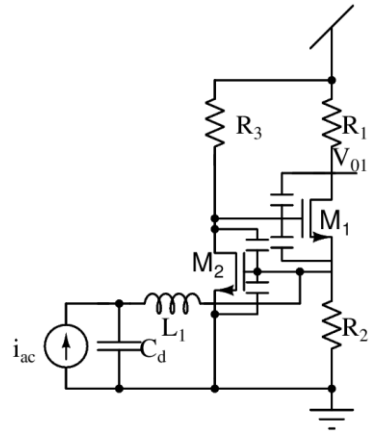

Fig.2 Circuit Diagram for RGC Stage

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In the proposed design a RGC network is inserted between the input of differential amplifier and photodiode to attain wide band response. RGC is essentially a common gate amplifier with a local feedback. In the proposed architecture as depicted in Figure2, transistor M2 with resistor R2 forms the local feedback of RGC amplifier.

Local feedback herein acts as a common source amplifier which gets a small portion of input signal and creates a voltage at the gate of M1. This signal is amplified at the output of M1. Moreover, it increases the effective transconductance of common gate structure which reduces the input resistance [9,10]. Reduction in input resistance isolates the input pole associated with large parasitic capacitance, Cpd from the bandwidth determination. As a result, the dominant pole of TIA is located within the amplifier rather than at the input node. To increase the bandwidth more, shunt peaking inductor LD1 and series peaking inductor LS1 are also incorporated in the RGC structure. These inductors are chosen similar to the technique described for the peaking inductors of differential amplifier.

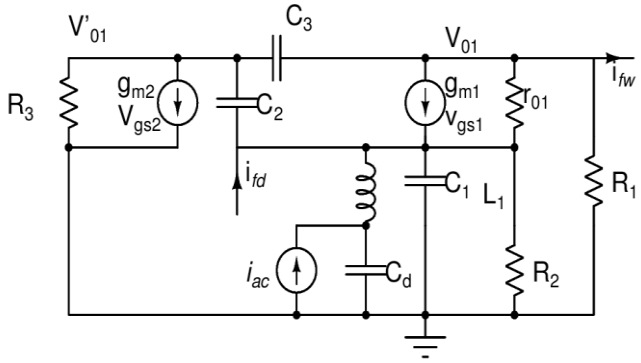

FIG.3 EQUIVALENT SMALL SIGNAL MODEL FOR RGC STAGE

Appling, the small signal analysis method for equivalent circuit. First, the redefine capacitance, gate to source capacitance of MOSFET 2 is denoted as C1, gate to source capacitance of MOSFET 1 and gate to drain capacitance of MOSFET 2 is denoted as C2, and gate to drain capacitance of MOSFET 1 is denoted as C3.

$$C_1 = C_{gs_2},\ C_2 = C_{gs_1} + C_{gd_2}, C_3 = C_{gd_1} \quad (1)$$

First, calculate gate to source potential of MOSFET 1 and MOSFET 2

$$V_{gs_1} = V'_{0_1} - V_1,\ V_{gs_2} = V_{0_1} \quad (2)$$

Now, the apply small signal model and finding transimpedance and calculating V_{01}, so at node V'_{0_1} is

$$\frac{V'_{0_1}}{R_3} + g_{m_2}V_{gs_2} + SC_2(V'_{0_1} - V_1) + SC_3(V'_{0_1} - V_1) = 0 \quad (3)$$

At node V_{o_1}, we getting

$$i_{fw} + \frac{V_{0_1}}{R_1} + \frac{V_{0_1} - V_1}{r_{o_1}} + g_{m_1}V_{gs_1} + SC_3(V_{0_1} - V'_{0_1}) = 0 \quad (4)$$

At node V_1, we also getting

$$(V_1 - V'_{0_1})SC_2 - g_{m_1}V_{gs_1} + \frac{(V_1 - V_{0_1})}{r_{o_1}} + \frac{V_1}{R_2} - i_{fb} + V_1SC_1 - i'_{ac} = 0 \quad (5)$$

$$V_d = \left(i_{ac} + \frac{V_1}{SL_1}\right)\left(\frac{SL_1}{1 + S^2L_1C_d}\right) \quad (6)$$

From eq.5 and eq. 6, we getting

$$V_1\left[SC_2 + \frac{1}{r_{o_1}} + \frac{1}{R_2} + SC_1 + \frac{1}{SL_1} - \frac{1}{SL_1(1 + S^2L_1C_d)}\right] - \frac{V_{0_1}}{r_{o_1}} - i_{fb} - \frac{i_{ac}}{(1 + S^2L_1C_d)} - V_{0_1}g_{m_1} + V_1g_{m_1} = 0 \quad (7)$$

By solving above equation, we getting

$$V'_{0_1}\left(SC_2 + SC_3 + \frac{1}{R_3}\right) + V_{0_1}(g_{m_2} - SC_3) - SC_2\left[V_{0_1}\left(\frac{1}{r_{o_1}} + gm1 + ifb - iac1 + S2L1Cd * ro1R2ro1R2SC1 + SC2 + gm1 + SCd + ro1 + R2 = 0\right.\right. \quad (8)$$

Here, we neglecting $r_{o_1} and R_2$ because the product of r_{o_1}, $R_2 and g_{m_1}$ is very large

$$V'_{0_1}\left(SC_2 + SC_3 + \frac{1}{R_3}\right) + V_{0_1}(g_{m_2} - SC_3) - \left[V_{0_1}\left(\frac{1}{r_{o_1}} + gm1 + ifb - iac1 + S2L1Cd * SC2SC1 + SC2 + gm1 + SCd = 0\right.\right. \quad (9)$$

Again arrange equations, we get

$$i_{fw} + V_{0_1}\left(\frac{1}{R_1} + \frac{1}{r_{o_1}} + SC_3\right) + V'_{0_1}(g_{m_2} - SC_3) - \left(\frac{1 + g_{m_1}r_{o_1}}{r_{o_1}}\right)\left[\frac{1}{(SC_1 + SC_2 + g_{m_1} + SC_d)}\right] * \left[V_{0_1}\left(\frac{1}{r_{o_1}} + g_{m_1}\right) + i_{fb} + iac1 + S2L1Cd = 0\right. \quad (10)$$

After simplifies above mention equation, we get

$$i_{fw} + V'_{0_1}(g_{m_2} - SC_3) + V_{0_1}\left(\frac{1}{R_1} + \frac{1}{r_{o_1}} + SC_3\right) - \left(\frac{1 + g_{m_1}r_{o_1}}{r_{o_1}}\right)^2\left[\frac{1}{(SC_1 + SC_2 + g_{m_1} + SC_d)}\right] - i_{fb}\left(\frac{1 + g_{m_1}r_{o_1}}{r_{o_1}(SC_1 + SC_2 + g_{m_1} + SC_d)}\right) - \frac{i_{ac}(1 + g_{m_1}r_{o_1})}{r_{o_1}(1 + S^2L_1C_d)(SC_1 + SC_2 + g_{m_1} + SC_d)} = 0 \quad (11)$$

After manipulating equations, we got

$$i_{fb}g_{m_1}R_1 + i_{ac}\frac{g_{m_1}R_1}{(1 + S^2L_1C_d)} - i_{fw}(g_{m_1} + SC_d)(1 + SR3C2R1 + V01gm12gm2R1R3 + gm1gm2R1R3SCd - S2CdC2R3 - S2CdC3R3R1gm1 = 0 \quad (12)$$

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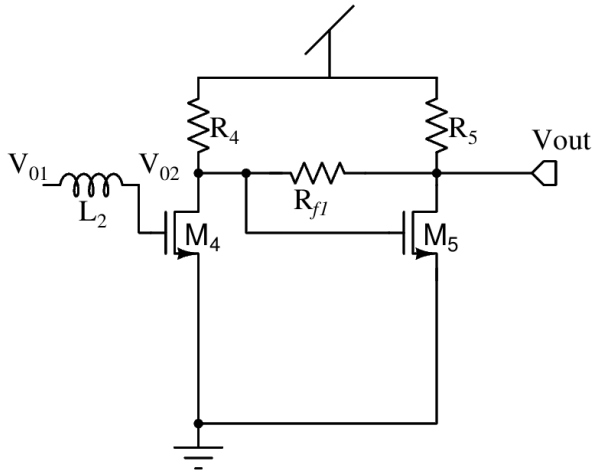

Fig.4 Common Source Amplifier's Circuit Diagram.

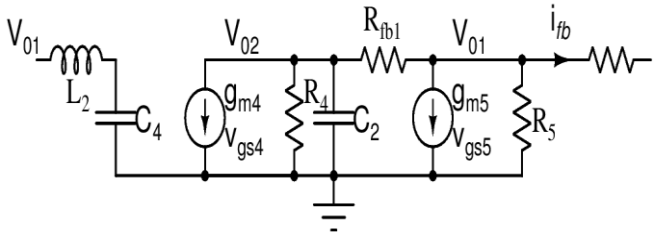

Fig.5 Common Source Amplifier's Small Signal Model.

Now, applying nodel analysis at node V_{0_2}& find the V_1

$$V_1 = \frac{g_{m_1}+SC_d}{1+R_{f_{b_2}}(g_{m_1}+SC_d)(g_{m_1}+SC_d)}\left[g_{m_1}V_{0_1}R_{f_{b_2}} + V_O + \frac{i_{ac}}{(1+S^2L_1C_d)}\right] \quad (13)$$

After solving above equation, it's get below final result

$$\frac{V_O}{i_{ac}} = -\frac{\left[g_{m_1}{}^2 g_{m_2}R_1R_4g_{m_5}R_5R_{f_{b_2}}+SC_dR_4g_{m_4}g_{m_5}R_5R_{f_{b_2}}g_{m_1}R_1+S^2C_dC_2R_3R_5R_{f_{b_2}}\right]}{g_{m_1}R_1\left(g_{m_1}g_{m_4}g_{m_5}R_4R_5R_{f_{b_2}}+SC_dC_4R_4R_5g_{m_4}g_{m_5}R_{f_{b_2}}+S^2L_2C_4R_{f_{b_2}}R_5g_{m_1}+S^3L_2C_4C_dR_{f_{b_2}}R_4\right)} * \frac{R_{f_{b_2}}(g_{m_1}+SC_d)}{(1+S^2L_1C_d)(1+S^2L_2C_4)} \quad (14)$$

Equation17 is similar to Inverse-Chebyshev/Elliptic filter which is having some transmission zeros. From equation17, it can say if there are doing proper tuning of inductor L1 and L2 then we get poles in the pass band so we can able to maximize the bandwidth. It is know that the Gain Bandwidth product is constant, so we can put feedback resister Rfb1 and Rfb2 so this is reduce gain and maximize operating frequency.

The maximum frequency also dependent in MOSFET fabrication process Technology. The f_T of MOSFET dependent of Technology. In this design using two negative feedback for enhanced the bandwidth. The operating bandwidth also dependent on the photo diode capacitor so it can resonant out that capacitor.The gain of circuit dependent of gm of MOSFET which is dependent on size of MOSFET. If whenever increasing the size of MOSFET then it is getting heavy input gate capacitance of MOSFET. So this design is optimize the size of MOSFET, inductor size, photo diode capacitor, feedback resistor, etc.

III. SIMULATION RESULTS WITH ENHANCE BANDWIDTH TRANSIMPEDANCE AMPLIFIER

Simulation Environment

The proposed TIA is designed in 130nm CMOS technology with 1.2 V supply voltage. RF NMOS and PMOS transistors are used for high frequency operation. The Photodetector capacitance is emulated using 60 fF MIM capacitor, and spiral inductors are used as peaking inductors. The whole system is characterized in SPECTRE/SPICE environment.

Transimpedance Gain Responses

The SPECTRE/SPICE simulation of transimpedance gain response is shown in Figure7 Transimpedance gain response is investigated in three different scenarios - when there is no compensation, compensation with degenerating capacitance and feedback network and compensation with degenerating capacitance, feedback network, and peaking inductors.

The below figure 7 shows the gain variation with respect to frequency. It also uses feedback resistors with large value. In this figure, it again marked at different gain.

The first point shows gain from dc to 100MHz which is 66.56 dB. Due to pole placement, it is able to achieve high bandwidth. The second point at 3.63GHz shows the gain at dip is 64.32dB due to effect of pole but it also cancel this pole with zero so the third point at 6.31GHz shows the overshoot and gain is 66.03dB.

The forth point shows 3-dB cut-off frequencywhich is 7.5GHz. The above discussed result is using large value of feedback resistors or it can say this circuit is without feedback resistors. If it is using a low value resistor then it can found large bandwidth and less gain.

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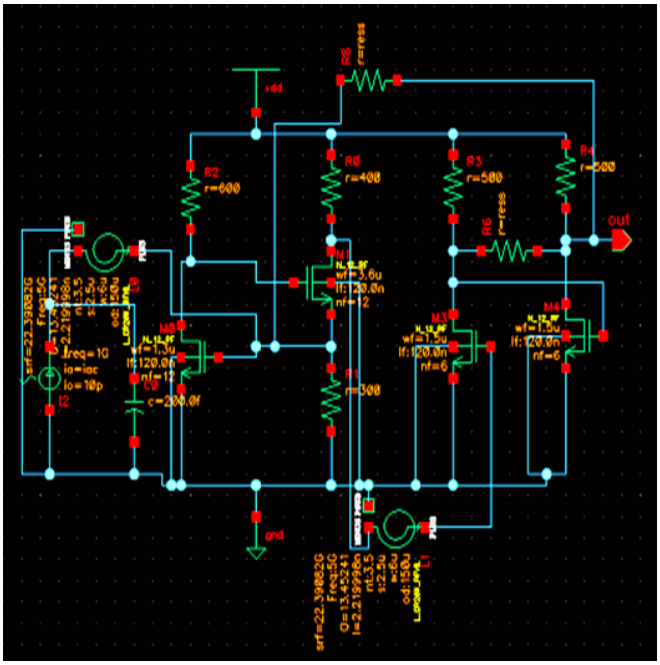

Fig.6Schematic Diagram in Software (Cadence Virtuoso or T-Spice).

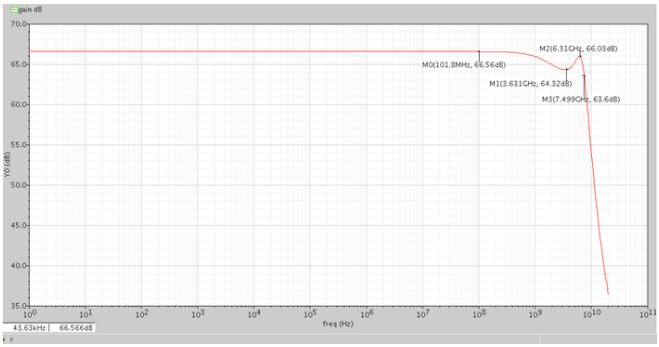

Fig.7Gain V/S Frequency Plot for TIA.

From below figure it is seen that if we are using small feedback resistor then gain is dramatically decreases and 3dB bandwidth is slightly increases. So it can use variable resistors so it can manage gain as well as bandwidth according to requirement of application.

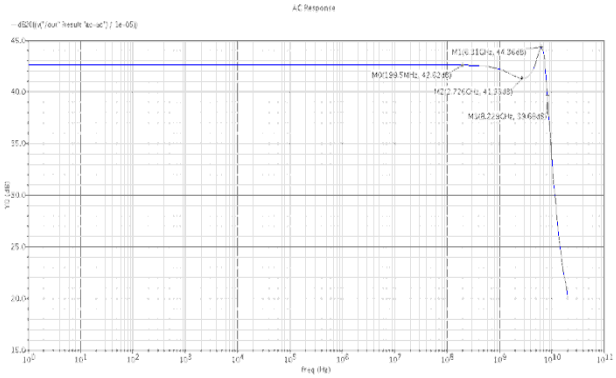

Fig.8 Gain V/S Frequency Plot for RGC Stage.

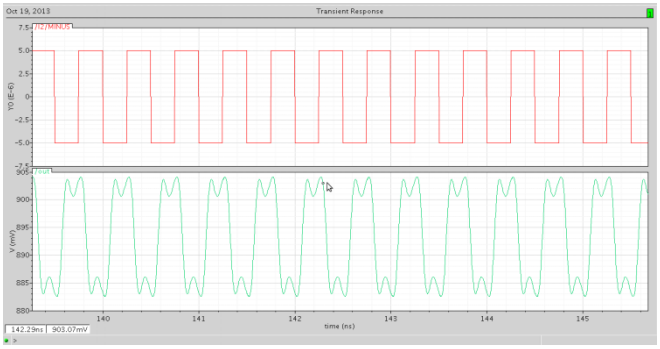

Fig.9 TIA Time Domain Output at 2GHz.

The above figure shows that the input is applied is square wave pulse then the output is distorted because the high speed input is faded into circuit and output is not settled but next input pulse also applied so we can see distorted wave. The below figure shows clear picture of output settling

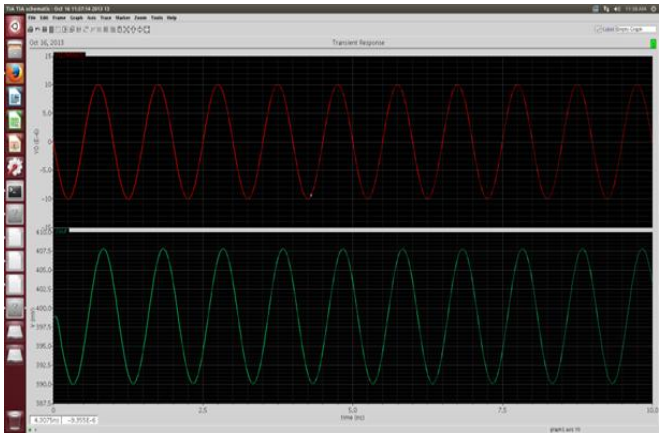

Fig.10 TIA Time Domain Output at 25GHz.

He below figure shows if we are applying very high frequency the output not settled so we can show a nearly sinusoidal wave. If it is apply very high frequency the output is completely distorted and unable to detect output.

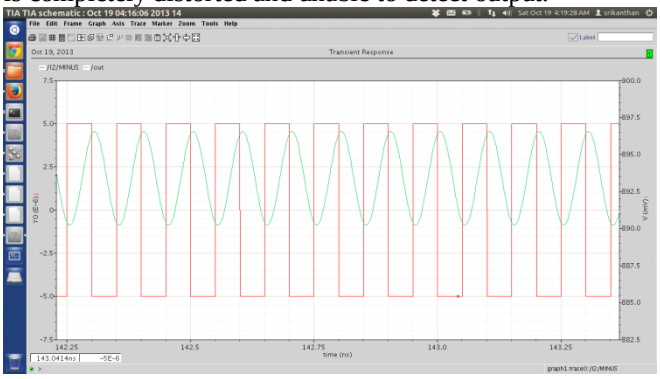

Fig.11 TIA Time Domain Output at 33GHz

For the variable gain and bandwidth requirement we can use MOSFET as variable resistor. The many non idealities come into picture such as the finite quality factor of inductors,

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non-ideal behaviour of photo diode, and non-ideal performance of MOSFET etc. Due to non-ideal behaviour we are facing problems such as harmonics, poor phase noise, high leakage current etc.

Performance of Proposed TIA

In this section, the performance issue discussed the proposed architecture of TIA over the available TIA with CMOS technology. The proposed architecture also marks a sharp difference with other TIAs by 40Gb/s data rate[8]. These TIA architecture achieves highest bandwidth and lowest group delay variation among all the TIA architectures. Input referred noise of proposed TIA is in between all of the architectures. Power consumption is the second lowest which also provides a decent figure of merit.

IV. CONCLUSION

This work provides an overview of the existing transimpedance amplifiers in CMOS technology to enhance the bandwidth of TIA architecture so that it can be operated in 40Gb/s data rate over the 10Gb/s data rate. It is also trade-offs between gain, bandwidth, noise, and group delay variation introduce severe hindrances to attain optimum performance of the TIA. Different TIA architectures such as improved RGC, RTRN network, nested feedback etc. are studied in detail to improve the frequency response of the TIA. The proposed TIA is based on differential architecture with an RGC network as input and incorporating a feedback network and peaking inductors for bandwidth enhancement. Capacitive degeneration is also introduced to increase the number of zeros for better phase performance. Total system has been analyzed for transimpedance gain response and noise performance. From simulation results, the proposed architecture shows excellent performance in terms of bandwidth and group delay variation with good transimpedance gain, input referred noise, and power.

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